

December 17, 2003

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/679,736 10/06/03

Yeung-Way Teh et al.

A NOVEL COPPER METAL STRUCTURE FOR THE REDUCTION OF INTRA-METAL CAPACITANCE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

CS-00-153CB

- U.S. Patent 5,109,267 to Koblinger et al., "Method for Producing an Integrated Circuit Structure with a Dense Multilayer Metallization Pattern," discloses a sloped metallization.
- U.S. Patent 5,821,141 to Huang, "Method for Forming a Cylindrical Capacitor in DRAM Having Pin Plug Profile," discloses a capacitor with a rounded top opening.

The following three U.S. Patents disclose interconnect shaped and processes:

- 1) U.S. Patent 4,888,087 to Moslehi et al., "Planarized Multilevel Interconnection for Integrated Circuits."
- 2) U.S. Patent 6,114,243 to Gupta et al., "Method to Avoid Copper Contamination on the Sidewall of a Via or a Dual Damascene Structure."
- 3) U.S. Patent 6,103,619 to Lai, "Method of Forming a Dual Damascene Structure on a Semiconductor Wafer."

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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